

Novel Cascadable Magnetic Majority Gates for Implementing Comprehensive Logic Functions

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Abstract—In the quest for novel, scalable and energy-efficient computing technologies, spin-based logic devices are being extensively explored due to their potential for nonvolatility, small cell area, and low operational power. Spin torque majority gate (STMG) is one of the most promising options for beyond CMOS nonvolatile logic circuits for normally-off computing. However, significant problems arose with cascade-ability, signal nonreciprocity, and complicated circuit configurations based on STMG. In this paper, a novel magnetic majority gate (MMG) logic has been proposed, utilizing both spin transfer torque and spin-orbit torque effects. A logic family including and/nand and or/nor functions can be achieved with an easy configuration and under a stable operation. Communication between logic units is realized by spin current injection through a non-ferromagnetic metal wire to ensure its cascade-ability and nonreciprocity to design multiple logic-depth circuits. With all of these advantages, the proposed cascadable MMGs can be utilized to design logic functions such as the BUFFER/NOT, XOR/XNOR, and complicated logic gates, which pave the pathway for designing robust and comprehensive logic circuits using full spintronic devices.

Index Terms—Beyond-CMOS logic devices, cascading, magnetic majority gates (MMGs), magnetic tunneling junction (MTJ), micromagnetic simulations.

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I. INTRODUCTION

SPIN logic (*a.k.a.* spintronic) circuit is a promising candidate for the beyond-charge-based computing scheme, due to its data nonvolatility and low operational power. So far, proposed spin logic devices include nanomagnetic logic [1]–[7], all-spin logic (ASL) [8], [9], magnetic tunneling junction (MTJ) integrated with CMOS logic [10], spin torque majority gates (STMGs) [11]–[17], mLogic [18], spin transfer oscillator logic [19]–[22], the spin wave bus devices [23], [24], and the spin transfer torque (STT) triad [25]. In particular, spin logic devices are amenable to building majority gates in which the circuit complexity is largely reduced due to the device counts decrease significantly as compared to other logic styles [11]–[17].

In principle, three vital features are necessary for pragmatic logic circuit implementations, namely, the completeness for Boolean operations, cascade-ability, and nonreciprocity. Conventional STMG designs have several shortcomings such as the oscillatory switching behavior [11] and the signal backward propagation [15], which lead to a narrow operating window of the circuits [14]. The inverting (*i.e.*, NOT) function in STMG is implemented based on a rather complicated structure, in which two ferromagnetic (FM) co-layers connected by a thin ruthenium spacer are utilized as the free layer [16]. The inflexible inverter topology makes the STMG difficult to constitute complicated logic functions [15], [16]. To address the aforementioned challenges, device structures such as the cascade-able STMG [12], [15] and the ASL [8], [9] satisfy the logic tenets above have been proposed [8]. For example, a robust design based on STMG [12] could mitigate the instability problems by setting pinning sites. However, the inverter part of the device is moved to the circuit's input terminals, which is not an ideal solution in the perspective of circuit cascade-ability. In ASL, the embedded insulating regions in the channel, which is utilized to prevent back current flow from output to input, complicate the fabrication process [8], [9]. Furthermore, these two designs are not favorable for device area scaling [26].

In this paper, a novel cascadable magnetic majority gate (CMMG) logic is proposed based on both STT and spin-orbit torque (SOT) effects in the MTJ and associated structures. The basic logic unit consists of a T-shaped, extended free layer shared by four MTJs as their bottom FM electrode.

The magnetization of the free layer can be switched via STT carried by the injected current. The output terminal locates at the joint of three input-MTJ branches, so that its magnetization can be determined by the propagation of magnetic domain walls (DW) without retreat or reflection effects. The NOT gate can be simply implemented through the switching of fixed layer's magnetization via SOT effect. Communication between logic units is realized by nonlocal spin diffusion current (similar to the mechanism used in ASL [8], [9]) through a non-FM metal wire to ensure its cascade-ability and signal nonreciprocity. Comprehensive logic functions including NAND/AND, NOR/OR, and XOR/XNOR are designed, together with the demonstration of their successful cascade-ability to implement complicated logic functions. This newly proposed magnetic device structure is more compatible with CMOS manufacturing process, as compared to existing STMG and ASL structures. The micromagnetic simulations are performed in this paper to evaluate the CMMG device, circuit performance, and energy consumption based on pragmatic technology.

II. MODELING AND SIMULATION

Magnetization dynamics are simulated to evaluate the switching process in the extended free layer of the CMMG. The object-oriented micromagnetic framework (OOMMF) [27] toolkits have been used, which solve Landau–Lifshitz–Gilbert (LLG) equations for FM medium. The Slonczewski-type STT and spin-hall effect-induced SOT were further implemented into OOMMF according to [28]

$$\frac{d\hat{m}}{dt} = -\gamma \hat{m} \times \vec{H}_{\text{eff}} + \frac{\alpha}{M_s} \hat{m} \times \frac{d\hat{m}}{dt} + \tau_{\text{STT}} + \tau_{\text{SOT}}$$

where

$$\vec{H}_{\text{eff}} = \frac{K_u}{M_s} \hat{z} + \frac{2A_{\text{ex}}}{M_s^2} \cdot \nabla^2 \hat{m} - 4\pi M_s \cdot D_{\text{ZZ}} \cdot \hat{z} + \vec{H}_{\text{ext}}$$

$$\tau_{\text{STT}} = -\frac{b_J}{M_s^2} \hat{m} \times \hat{m} \times (\hat{J}_e \cdot \nabla) \hat{m} + \frac{\xi b_J}{M_s} \hat{m} \times (\hat{J}_e \cdot \nabla) \hat{m} \quad (1)$$

where

$$b_J = \frac{P \cdot J_e \cdot \mu_B}{e \cdot M_s} \quad (2)$$

$$\tau_{\text{SOT}} = \frac{\theta_{\text{SH}} \cdot J_{\text{SH}} \cdot \mu_B}{e \cdot M_s \cdot L_z} \hat{m} \times \hat{m} \times \hat{z}. \quad (3)$$

Key contributing terms of the LLG equation are shown in (1). \vec{H}_{eff} refers to the effective magnetic field, including uniaxial anisotropy, exchange coupling, demagnetization, and Zeeman effects. \hat{m} is the normalized magnetization vector for the extended free layer, γ , α , D_{ZZ} , and \vec{H}_{ext} are Gyro-magnetic ratio, Gilbert damping constant, demagnetization coefficient along easy (z -)axis, and external magnetic field. The STT effect can be modeled using (2), where J_e , ξ , P , μ_B , and e are the current through MTJ, the ratio between Slonczewski and field-like torques, the spin polarization of the fixed layer, Bohr magneton, and elementary charge, respectively. The SOT effect is further described by (3), in which J_{SH} , θ_{SH} , and L_z stand for injected current to induced SOT, the spin-hall angle, and thickness of the heavy metal layer.

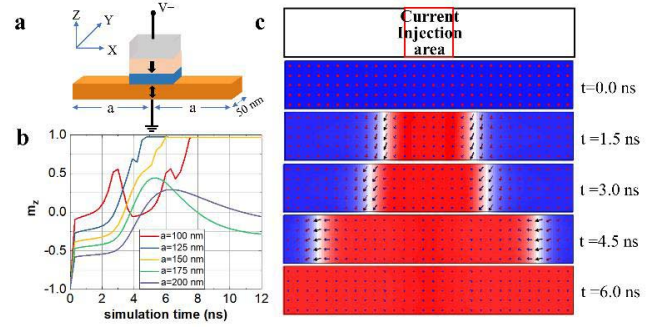


Fig. 1. (a) MTJ device with an extended free layer of length $2a$. The MTJ stack has a cell size of $50 \text{ nm} \times 50 \text{ nm}$ that locates in the center of the free layer. (b) Snapshots of perpendicular magnetization (m_z) at different time steps during the switching process. Red regions represent magnetization upward and blue regions represent magnetization downward. (c) Simulation results of the structure in (a) with various free layer lengths. The current stimulus is turned OFF at $t = 6 \text{ ns}$.

The saturation magnetization (M_s), exchange constant (A_{ex}), magnetic anisotropy energy density (K_u), spin polarization (p), and Gilbert damping constant (α) values used in this paper are $0.86 \times 10^6 \text{ A/m}$, $30 \times 10^{-12} \text{ J/m}$, 0.84 MJ/m^3 , 0.6 , and 0.014 , respectively, for the free layer, consistent with CoFeB-based FM material properties [29], and are $0.86 \times 10^6 \text{ A/m}$, $30 \times 10^{-12} \text{ J/m}$, 3.5 MJ/m^3 , 0.45 , and 0.014 , respectively, for the fixed layer. The thicknesses of the free layer and fixed layer are 2 and 2 nm . The mesh sites used in the numerical simulations are $1 \text{ nm} \times 1 \text{ nm} \times 1 \text{ nm}$ cubes. All of the FM layers are assumed to have perpendicular magnetization anisotropy (PMA), which shows better scaling promise for the state-of-the-art MTJ technology [29].

III. RESULTS AND DISCUSSION

A. MTJ With an Extended Free Layer

A PMA MTJ with extended free layer structure is shown in Fig. 1(a). The magnetization of the free layer can be switched by spin-polarized current even though the free layer is longer than the width of the MTJ. Under positive voltages, current flows from the fixed layer to the free layer, aligns their magnetizations in the antiparallel configuration (logic state “1”), while under negative voltages, current flows from the free layer to the fixed layer, aligns their magnetizations in the parallel way (logic state “0”). Dynamic switching process in the case of $a = 150 \text{ nm}$ with current density $J = 200 \text{ MA/cm}^2$ is shown in Fig. 1(b). It is clear to see that the switching boundary in the free layer extends beyond the MTJ stack's area where spin-polarized current flows perpendicularly, along the DW propagation [30]. Simulation results for various lengths of the extended free layer are summarized in Fig. 1(c), in which one can see that the averaged magnetization of the extended free layer fails to switch when its half-length (a) is longer than around 175 nm , due to the DW blocking effect determined by the FM layer's pinning potential [31]. In the process of DW automation, problems such as reflection and backward propagation of DW appear in long strip structures [32]. This undesirable feature can be explained by the demagnetization field, which depends on the geometry

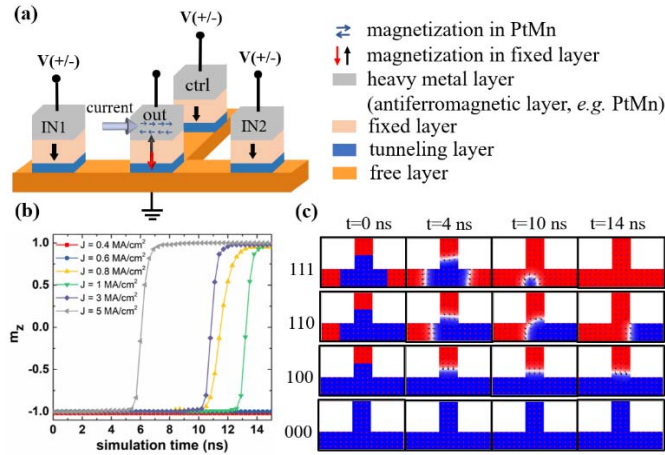


Fig. 2. (a) MMG unit structure. (b) Average magnetization of the output-MTJ's free layer with various current densities. The current stimulus is turned OFF at $t = 6$ ns. (c) For four states: 111, 110, 100, and 000 (three digits represent states of ctrl, IN1, and IN2, respectively), simulation of magnetization vary with time during the process is shown in four respective rows. Operational results of inputs obey the majority principle.

aspect-ratio of the free layer and is generated in the inter-connect region.

B. Implementation of and/or and nand/nor Gates

Based on the extended MTJ structure, the overall structure for the magnetic majority gate (MMG) unit cell is shown in Fig. 2(a), which consists of a T-shaped extended free layer and four MTJs, each of which has a cell size of $50 \text{ nm} \times 50 \text{ nm}$, and a thickness of 2 and 2 nm for free and fixed layers, respectively. Input-MTJs are located in the three branches of the MMG's extended layer, while the output-MTJ is located at the joint of these branches. During MMG's switching, out-of-plane current flows through the fixed layer of input-MTJs to switch the magnetization of their shared free layer via STT. In free layer's regions that are not contacted with MTJs, the magnetization is mainly driven by the short-range exchange coupling field [12]. The output state of MMG is detected by the fourth MTJ (output-MTJ) via the tunnel magnetoresistance effect. Note that the MMG can only work if the four MTJs are close enough to each other [as suggested by Fig. 1(c)]. In the case that the spacing between input-MTJs and the output-MTJ is beyond the exchange coupling field's range, when the DW reaches the center of the shared free layer, the input-MTJ may lose the interactions with the output-MTJ. With proper designs in this paper, such consequences can be avoided.

To implement the "AND" and "OR" logic functions, any of the three input-MTJs can serve as a control terminal, and it is reconfigurable. To be specific, when one input-MTJ (control terminal) is set as "1," the MMG performs the function of "OR" on the bottom two input-MTJs; otherwise, if one of the input-MTJ (control terminal) is set as "0," the "AND" function is realized. Simulated average magnetizations of the output-MTJ's free layer are shown in Fig. 2(b) and (c).

The implementation of NOT gates can be achieved with the help of SOT and antiferromagnetic (AFM) effects in the output-MTJ's fixed layer. With an AFM layer (e.g., PtMn)

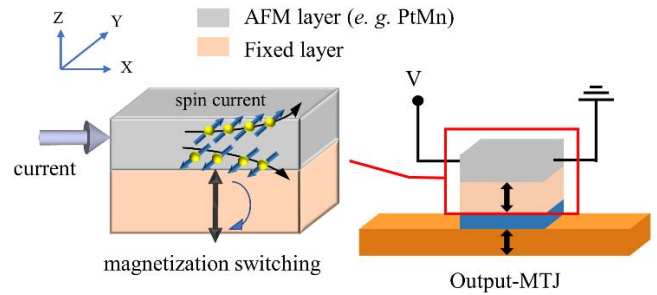


Fig. 3. Illustration of the output MTJ with AFM layer (e.g., PtMn) on the top of the fixed layer. The magnetization of the fixed layer can be switched by the SOT generated by the in-plane current and the exchange bias from the AFM layer.

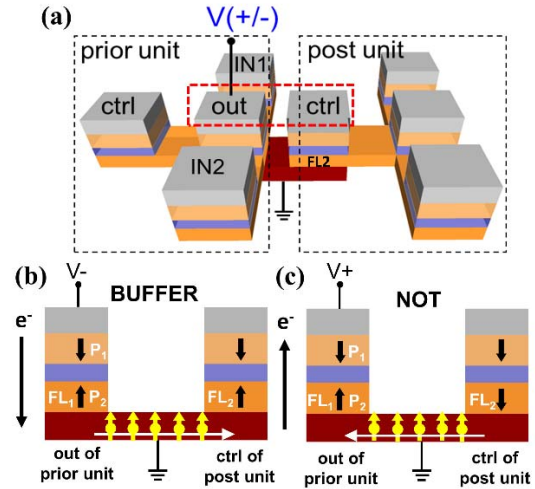


Fig. 4. (a) Illustration of two cascaded MMGs. The red region represents the copper wire. Implementations of the (b) "BUFFER" and (c) "NOT" gates, controlled by the voltage polarity of the prior unit's output.

directly attached on the top of the fixed layer, in-plane spin current (polarized along $+y$ or $-y$ direction) can switch the magnetization of the fixed layer's magnetization of the output-MTJ with joint effects of SOT and the exchange bias [33], as shown in Fig. 3. Spin current along the " $-y$ ($+y$)" direction can switch the magnetization of the fixed layer from up (down) to down (up) directions. As a result, the magnetization alignment between fixed and free layers changes from parallel to antiparallel (or vice versa). Therefore, the lack of inverter logic styles in STMG structures [12], [15] can be mitigated, so that "NAND" and "NOR" functions can be implemented in one single MMG. To achieve better thermal stability, the fixed layer could be designed as an synthetic antiferromagnetic stack [34] for practical applications.

C. Cascade-Ability and Implementation of xor/xnor Gates

The CMMGs are realized by a copper wire with long spin diffusion length (of around 500 nm at room temperature [35]) through nonlocal spin diffusion effects, as shown in Fig. 4(a). An isolation region embedded in the channel is required to implement the nonreciprocity in ASL; however, in the proposed CMMG, copper wire (channel) only serves as a bridge to connect the output-MTJ of the prior unit and one

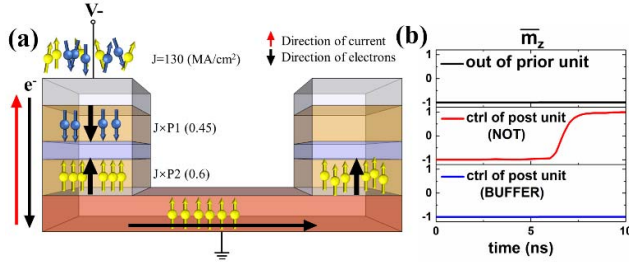


Fig. 5. (a) With negative voltages applied on the output-MTJ of prior MMG unit, current flows from the free layer to the fixed layer. Spin diffuses from the prior MMG unit to the post MMG unit through the copper wire, leading to a parallel state of the free layers and transferring logic state from the prior unit to the post unit. (b) Average magnetization of the output-MTJ's free layer in the prior unit and control-MTJ's free layer in the post unit for the "BUFFER" and "NOT" gates.

input-MTJ of the post unit, which further simplifies the device structure. Negative voltages applied on the output-MTJ would transfer an identical logic state of the prior unit to the post unit under sufficient high voltage, acting as a "BUFFER" gate, as shown in Fig. 4(b). While positive voltages applied on the output-MTJ would inverse a logic state from the prior unit to the post unit, acting as a "NOT" gate, as shown in Fig. 4(c).

The conditions of two MMGs can form good cascade-ability that are further discussed herein. As shown in Fig. 5(a), assuming spin polarizations of fixed layers and free layers are P_1 and P_2 , respectively, when the switching current J flows in the output-MTJ from the free layer to the fixed layer, it is first polarized by the fixed layer (due to electrons are injected from it). Therefore, spin-polarized current $J \cdot P_1$ is collected by the free layer of the prior unit's output-MTJ. If $J \cdot P_1$ is smaller than a critical switching current of the free layer (FL₁), the logic state of output-MTJ is maintained. The current afterward polarized by the free layer of output-MTJ; namely, spin-polarized current $J \cdot P_2$ will diffuse to the post unit's input-MTJ through the copper wire. If $J \cdot P_2$ is larger than the critical switching current of the free layer (FL₂), the spin-polarized current can switch the magnetization of input-MTJ in the post unit. As a result, the logic state of the post unit's input-MTJ is always the same as that of the prior unit's output-MTJ. On the other hand, when the current J flows in the output-MTJ from the fixed layer to the free layer, in a similar way, an adverse magnetization of output-MTJ can be transferred to post unit's input-MTJ, and its logic state is inverted. These conditions can be summarized as follows (under macrospin picture):

$$J \cdot P_1 \leq \frac{A\alpha M_S t_{FL}}{g(\theta)} (H_K - 4\pi M_S - H_{app} - H_{stray})$$

$$J \cdot P_2 \geq \frac{A\alpha M_S t_{FL}}{g(\theta)} (H_K - 4\pi M_S - H_{app} - H_{stray}). \quad (4)$$

If one assumes $P_1 = 0.45$ and $P_2 = 0.6$ for all of the MTJs. The critical current density J_c for switching the input-MTJ in the post unit in our CMMG device is roughly 120 MA/cm^2 , so if the switching current satisfies $J_c < J < J_c \cdot (P_2/P_1)$ (i.e., from 120 to 160 MA/cm^2) as mentioned above, magnetic state of the output-MTJ can be only transferred to the post unit without any influence on the inputs of the prior unit to achieve good nonreciprocity. An average magnetization of the

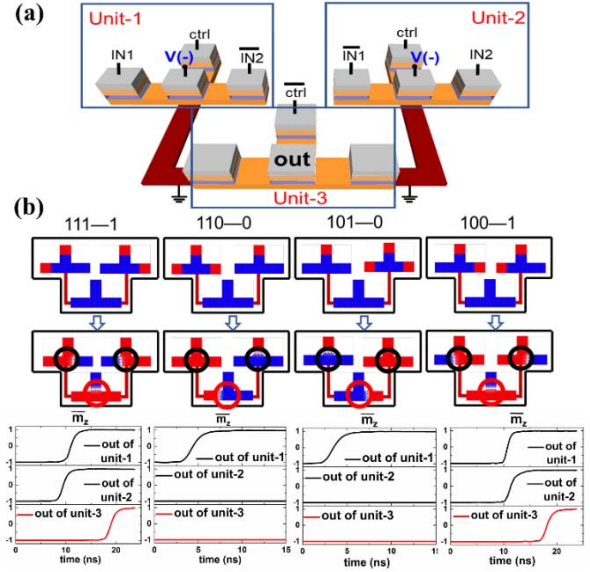


Fig. 6. (a) Implementation of "xor" and "nxor" based on CMMG. (b) Simulation of four cases in "xor" function and the average magnetization of the output-MTJ's free layer in unit-1, unit-2, and unit-3, respectively, corresponding to the circled area.

TABLE I
PERFORMANCE OF CMMG DEVICE

	①	②	③
Size of MTJ (nm ²)	50×50	25×25	20×20
Length of copper wire (nm)	140	90	56
Critical current density (MA/cm ²)	100	60	50
Current pulse duration (ns)	7.00	4.00	4.00

output-MTJ's free layer in the prior unit and control-MTJ's free layer in post unit is shown in Fig. 5(b).

The CMMG structure enables the implementation of "XOR" and "XNOR" functions as shown in Fig. 6(a) and (b). There are totally three MMG units involved, in which unit-1 and unit-2 deliver the intermediate results to feed into unit-3 for the final output. Constant negative voltage is applied onto the control-MTJ of unit-3. With the states of ctrl-MTJs set as shown in Fig. 6, output-MTJ of unit-1 delivers the result of "IN1" + "IN2" to one of the input-MTJs of unit-3 while the output-MTJ of unit-2 delivers the result of "IN1" + "IN2" to the other input-MTJ of unit-3, the function of ("IN1" + "IN2") · ("IN1" + "IN2") is thus calculated to fulfill the XOR function. Similar to the logic function selection between "AND" and "OR," if the control-MTJ is set at "1," the function of "XNOR" can be achieved. So far, all necessary logic components are implemented by the proposed CMMG devices and more complicated logic cells including AND-OR-inverter gates and full adders can be constructed in a straightforward way.

D. Scaling Studies on CMMG

Studies on the scalability of the proposed CMMG device have been performed to further evaluate their potentials in fabricating large-scale logic circuits. As shown in Table I,

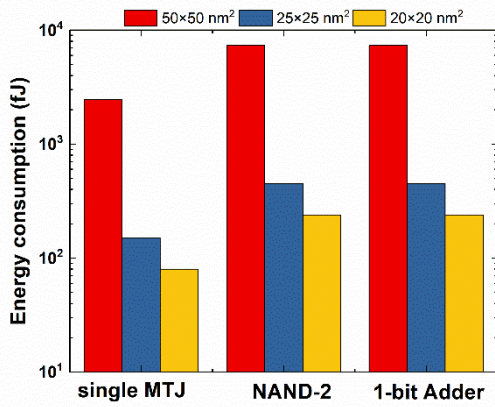


Fig. 7. Joule-heating-induced energy dissipation in the MMG-based circuits with different cell sizes.

TABLE II
COMPARISON OF DEVICE COUNTS TO IMPLEMENT
DIFFERENT LOGIC FUNCTIONS

	Device	INVFO4	NAND2	1-bit Adder	32-bits Adder
CMMG	1	1	1	3	96
CMOS	1	2	4	28	1344

the MTJ's cell size has been scaled down to $20 \text{ nm} \times 20 \text{ nm}$, together with the channel length to 16 nm (corresponding to $a = 8 \text{ nm}$ in Fig. 1). A decrease of the critical current density is seen with MTJ cell size scaling as shown in Table I. Due to the nonvolatile nature, the energy consumption for operating CMMG devices only consists of the dynamic part and is modeled according to the methodology proposed in [36]. Joule-heating-induced energy dissipation in the MTJ-stacks, copper wires, and AFM layers during switching is calculated with the operating V_{dd} down to 0.1 V ; the resistivity of copper wire is $1.75 \times 10^{-8} \Omega \cdot \text{m}$ and the resistivity of AFM layer is assumed to be $10 \times 10^{-8} \Omega \cdot \text{m}$. In the case that the MTJ stack's cell size of $20 \text{ nm} \times 20 \text{ nm}$, the energy dissipation of a NAND2 gate and 1-bit adder circuit is as low as 240 fJ . The total energy dissipation on CMMGs with different cell sizes is shown in Fig. 7, showing that the total energy consumption decreases with CMMG device area scaling. Note that, compared with the state-of-the-art CMOS technologies as provided in [36], the overall energy efficiency for either STMG or CMMG is still not very competitive. Material innovations on FM, exchange coupling, and spin diffusion layers are regarded as further action items to tackle this issue.

Table II illustrates the comparison of the device counts for various logic circuit designs based on CMMG and CMOS technologies. One can see that to implement an identical logic function, the number of devices used in CMMG is far less than that used in CMOS circuits. With increasing device integration, the much reduced device counts of CMMG are expected to be beneficial for reducing chip footprint. This results from the help that the fabrication of CMMG is within back-end-of-line technology layers, leaving extra the potential for 3-D monolithic integration schemes.

IV. CONCLUSION

In summary, a novel CMMG logic utilizing both STT and SOT to switch the device's magnetization state and designed cascade-ability is proposed. For the first time, complete logic family including AND/NAND, OR/NOR, XOR/XNOR, and BUFFER/NOT gates has been implemented in very straightforward ways, paving a pathway for designing complicated logic circuits. Physics-based micromagnetic simulations are performed on the above designs to estimate switching speed and energy dissipation. Results indicate that CMMG logic has comparable performance to existing MTJ and spintronic device technology, featuring high energy efficiency, together with the promising device scalability and easy for fabrication, CMMG is an excellent option for CMOS-replacement nonvolatile logic.

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